DIGITAL ACCELEROMETER WITH FEEDBACK CONTROL USING SIGMA DELTA MODULATION

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ABSTRACT

This paper describes a digital accelerometer implemented in a bulk micromachining technology. The accelerometer measures changes in a differential capacitance to detect deflections of a proof mass, which result from acceleration input. The differential capacitance is connected to position sense interface whose output is used for one bit force feedback. The heart of the feedback system is sigma delta modulation or over-sampling technique, which includes direct digital output signal and noise shaping properties. Open loop sensors are fabricated at ITIMS and the feedback system is designed in MATLAB.

1. INTRODUCTION

MEMS based accelerometer is one type of advanced sensors that applied widely to varied fields, such as automobile and household electronics [1]. The silicon capacitive accelerometers have several advantages that make them very attractive for many applications. They have high sensitivity, good DC response and noise performance, low drift, low temperature sensitivity and low power dissipation. Furthermore, additional capacitors can be integrated and used in a closed-loop feedback configuration for electrostatic force rebalancing [2, 3].

Several different types of the open loop structures are fabricated in ITIMS but there is a great need for a closed loop accelerometer. This paper focus on design of the closed-loop force feedback structure incorporated in the sensor. By using the sigma-delta technique, we can get a direct digital output signal in form of a pulse density modulated bitstream which is suitable for digital processing, improves system stability and reduces the quantization noise by increasing the sampling frequency of the modulator. Sigma-delta converters have been receiving much attention recently in the VLSI industry. The early use of sigma-delta conversion was limited primarily to voice band codecs. There is now a growing potential for sigma-delta converters in such areas as communication systems, digital audio tape, compact disc and MEMS sensors. By applying delta-sigma modulation on MEMS accelerometers, it is possible to accomplish three tasks at once: producing high resolution digital output; providing feedback linearization to suppress sensor nonlinearities and variations; and applying closed loop control to reduce Brownian noise [4].

2. MEMS ACCELEROMETER

The accelerometer in Fig.1 is a vertical structure, which suggests the use of bulk micromachining. The bulk micromachined capacitive accelerometers provide larger proof mass and larger capacitive area that lead to a higher resolution and greater sensitivity. This silicon accelerometer consists of a proof mass (M) attached to a fixed frame by four suspension beams, which have an effective spring constant of K.

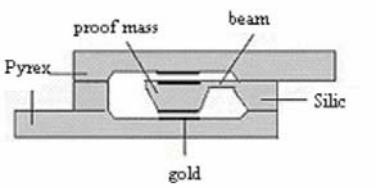

Fig. 1: General capacitive accelerometer

The operation of the device is based on Newton's second law of motion. An external acceleration results in a force being exerted on the mass. This force results in a deflection x of the proof mass, where a is the frame acceleration. The following second-order mechanical transfer function from acceleration to a displacement of the mass can be obtained:

$$H(s) = \frac{x(s)}{a(s)} = \frac{1}{s^2 + \frac{D}{M}s + \frac{K}{M}} = \frac{1}{s^2 + \frac{\omega_r}{Q}s + \omega_r^2} \qquad (1)$$

where $\omega_r = \sqrt{K/M}$ is the resonant frequency, D is damping factor and $Q = \omega_r M / D$ is quality factor.

Fig. 2 shows two different accelerometer structures fabricated at ITIMS [5]. These bulk capacitive accelerometers, which consist of a glass-silicon-glass wafer stack and two differential sense capacitors, are formed by aluminum layers.

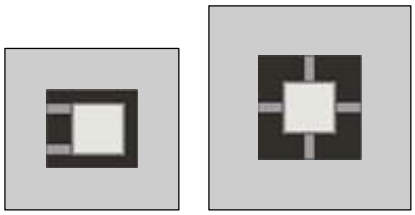

Fig. 2: Suspension structures: double spring beam (a) and four symmetrical spring beam (b)

Fig. 3 shows the frequency response of the open loop accelerometer that depends on damping factor D. We need our device to be critically damped (i.e. D=0.707) because when the system is critically damped, it has the least amplitude distortion, and the output follows the input over the widest frequency range. Unfortunately, it's quite difficult to control the damping effect, so it is suggested that we should use the closed loop accelerometer. Using closed loop accelerometers, we can overcome not only the damping problem but also other nonlinearity effects [6].

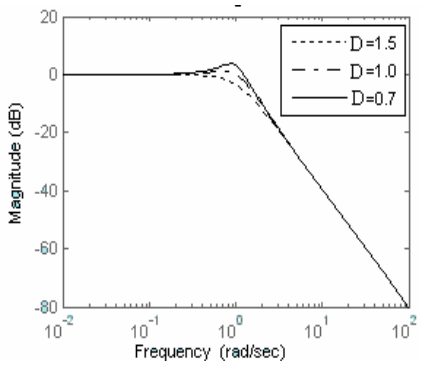

Fig. 3 Frequency response of the open loop accelerometer

3. SIGMA-DELTA MODULATION

Sigma-delta modulation is also called oversampling converter or charge balancing A/D converter. Sigma-delta converters differ from other ADC approaches by sampling the input signals at a much higher rate than the maximum input frequency. The ratio between the actual sampling rate (FS) and the Nyquist rate (2fmax) is referred to the oversampling ratio (OSR):

$$OSR = FS/2fmax \qquad (2)$$

Advantages of the oversampling converter are simplification of the anti-aliasing filter, support for anti-aliasing filtering with variable cutoff frequency and a reduction in the ADC noise floor by spreading the quantization noise over a wider bandwidth. This makes it possible to use an ADC with fewer bits to obtain the same SNR performance as a higher resolution ADC.

The root-mean-square (RMS) value of the quantization noise σ is given by:

$$\sigma = \frac{\Delta}{\sqrt{12}} = \frac{2^{1-N}}{\sqrt{12}} \qquad (3)$$

where Δ is the quantized step size and N is the ADC word length. We assume that the energy of the quantization noise is spread evenly from 0 to FS/2. We can compute the quantization noise Pc(f):

$$P_c(f) = \frac{\sigma^2}{F_S} \quad (4)$$

Thus, we can improve the resolution of the ADC by sampling the input data at a high rate to spread the quantization noise energy over a wider frequency band. It means that we can reduce the levels of noise in the band of interest.

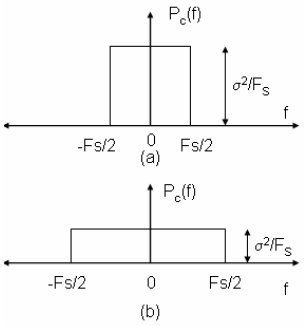

Fig. 4: Quantization noise power spectral density: (a) Nyquist rate converter (b) Oversampling converter

Fig.4 depicts the quantization noise power spectral density in two cases: Nyquist rate converter and oversampling converter. The total noise power is the same for both converters but the oversampling converters have the noise power distributed over a much wide frequency range leading to the smaller in-band noise power level.

3.1 The First Order Sigma-Delta Modulator

The block diagram of the first order sigma delta modulator is shown in Fig.5 which consists of an integrator, a comparator, which acts as an ADC and 1 bit DAC, which is placed in the feed back loop. The integrator accumulates the difference between the input and quantized output signals from the DAC output which is in feedback loop and makes the integrator output around zero. The integrator is the most important component in a sigma-delta modulator because it can shape the noise spectrum. Oversampling ADC usually uses switched capacitor techniques and hence do not use sample and hold circuits [7]. The output of the modulator is a pulse density modulated signal that represents the average of the input signal. The average of the output can be computed by a decimator filter. Fig.6 shows the SIMULINK model of the first order sigma delta modulator. The analog input and the quantized output are showed in Fig.7. We can observe that for the peak of the sine wave, most of the pulses are high and as the sine wave decreases in value, the pulses become distributed between high and low.

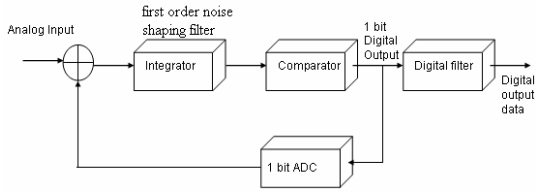

Fig. 5: A first order sigma delta modulator

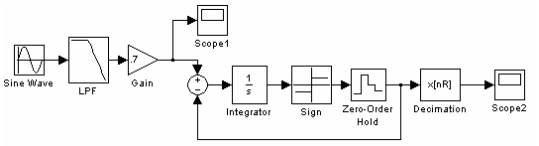

Fig. 6: SIMULINK model of oversampling single bit A/D conversion

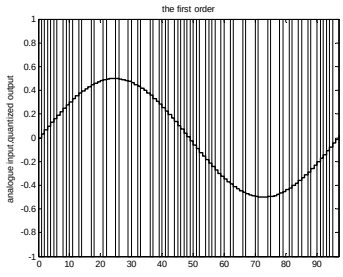

Fig. 7 Analog input and quantized output of the first order modulator (OSR=32)

3.2 The High Order Sigma-Delta Modulator

The performance of the sigma-delta modulator is depends on the forward path ADC resolution

(N), the OSR and the order of the modulator (i.e. number of integrators). The maximum signal to noise ratio (SNR) is given by [8]:

$$SNRmax = 1.76 + 6.02N + 10(2L+1)\log(OSR) + 10\log(2L+1) - 9.94L \quad (5)$$

Where N is the ADC word length (including single bit N=1) and L is the order of the modulator.

Single bit modulator has the advantage of better linearity and the OSR can not be too high due to circuit speed and power consumption constraints. For high resolution and high speed converters, high order modulators with more than two integrators are widely used. The stability of the high order modulators is a difficult problem. There are two popular architectures of high order modulators: interpolative architecture (see Fig. 8) and multi stage noise shaping (MASH) architecture (see Fig.9). The interpolative architecture implements a high order filter with the zeros of the noise transfer function spreading over the interested frequency band, thus, reduces the sensitivity to the component variations. The interpolative modulators must be carefully designed to ensure its stability [9]. The MASH structure constructs the high order modulators using the inherently stable first and second order loops, thus, ensures that the system is stable.

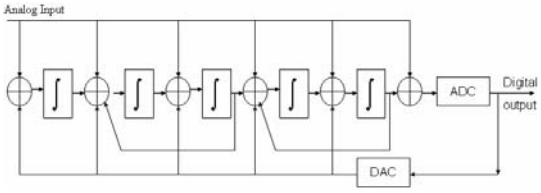

Fig. 8 Interpolative high order delta sigma modulator

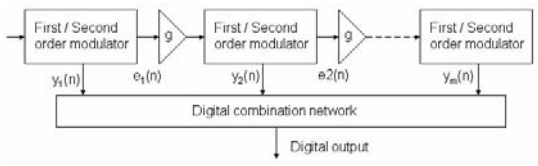

Fig. 9 MASH delta sigma modulator

3.3 Delta-Sigma Modulation in MEMS Based Accelerometer

Fig. 10 is the generic architecture of the sigma delta force balanced accelerometer. The open loop structure fabricated at ITIMS provides noise shaping (see Eq.1). High frequency sinusoidal signals are applied in anti phase to the top and bottom electrodes to determine the position of the proof mass. The amplitude of the signal from the seismic mass is measured by the imbalance in capacitance. Then, it is fed to a charge amplifier which is followed by a sample and hold circuit. The samples are achieved when the signal of the charge amplifier is at its peak. These discrete signals are fed to a comparator whose output is logic signal. If it is one, it implies that the seismic mass is above the central position between the two electrodes while a logic zero shows that it is below the centre position.

In the feedback path, the state of the comparator will determine a pulse whose constant voltage and constant duration is added to the high frequency excitation signal then applied to the electrode furthest away from the mass. The electrostatic force on the mass is mainly determined by the pulse of voltage because it is much greater than the excitation signal. Otherwise, the duration applied to an electrode is much longer than the period of the excitation signal.

The sampling frequency is much lower than the frequency of excitation signal because the charge amplifier output signal saturates on the leading and trailing edges of the feedback voltage pulse. This ensures that the sample occurs after the decay of the transient condition. We often choose a ratio of 10:1 between excitation and sampling frequencies.

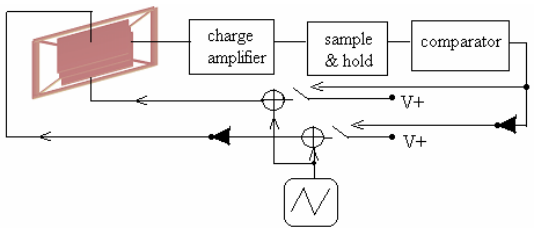

Fig. 10 Closed loop structure using sigma delta modulation

The mathematic model of the closed loop system is shown in Fig. 11. The model was written in MATLAB with M-file functions in which the voltage on the mass's electrode is sampled every T seconds (much faster than the required output of the digital signal), then filtered by a lead compensator Hc(z) (an FIR filter), and fed to an one-bit A/D converter. The filter Hc(z) provides compensation to the two pole mechanical structure to ensure the loop have sufficient stability. If Hc(z) contains L integrators, the modulator order is L+2. The outputs of the A/D converter are converted to force and fed back to the sensor. The linearity of the system is determined solely by the feedback, thus, is insensitive to the circuit imperfections on the forward path (i.e. the filter Hc(z) and the low resolution A/D). The outputs are also counted and averaged every N*T seconds to produce the digital output. In our program, the external acceleration is a 80 Hz sine wave whose range is ±1g.

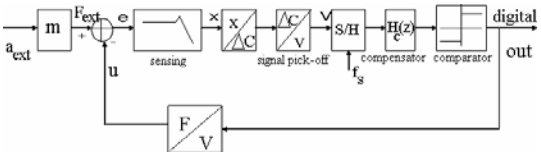

Fig. 11 The mathematic model of the closed loop system using delta sigma modulation

Fig. 12 shows the sinusoid acceleration input and the pulse density modulated output signal. In this simulation, the order modulator is 5, the oversampling rate is 32 and the external acceleration is a 80 Hz sine wave whose range is ±1g. This result agrees with the theoretical prediction.

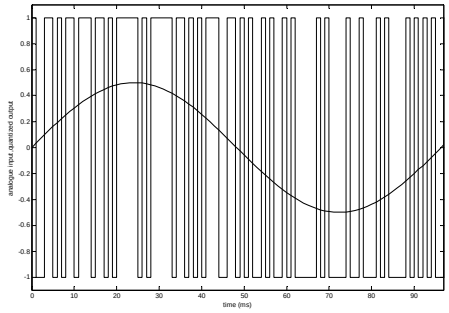

Fig. 12 Analogue input and digital output of the closed loop accelerometer

Fig. 13 depicts the spectrum of the digital output which acceleration signal's spectrum is separated. We can calculate the SNR is 82.5 dB and NBW is 0.00018. Putting bit stream into a decimation filter (i.e. computes the means of bit stream data), we can retrieve accurate signal (see Fig. 14).

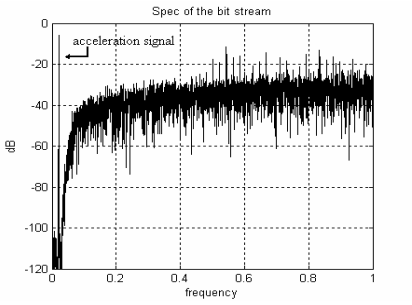

Fig. 13 Output signal's spectrum of the closed loop accelerometer

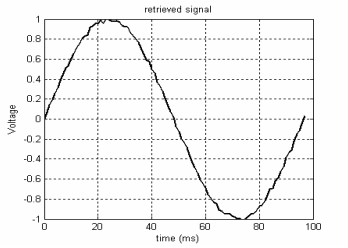

Fig. 14 Acceleration signal retrieved

Fig. 15 shows the simulation result for the unforced condition. It is easy to see that the mean of bit stream output is zero. It is our desired result in the unforced condition.

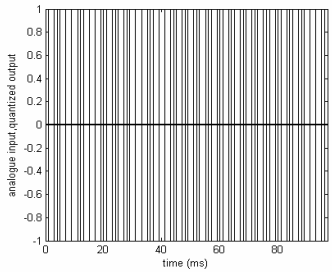

Fig. 15 Unforced condition (a=0)

Fig. 16 shows the static response of the sensor, which was rotated in the earth's gravitation field to generate acceleration from -1g to +1g. The linearity of the simulation is quite good and suitable to the desired result in this condition.

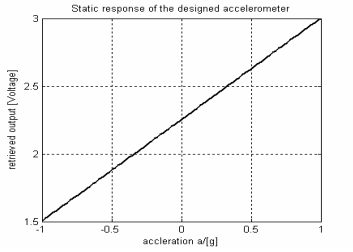

Fig. 16 Static response of the designed accelerometer

Table 1. Desired specification of the sensor and interface IC

Sensor Specification	
Device size	4mmx4mmx320µm
Sensitivity	0.4 pF/g
Brownian noise	$0.13\,\mu g/\sqrt{Hz}$
Resonant frequency	980 Hz
IC specification	
Sampling clock	20 kHz
Sensitivity	0.8 V/g
IC core size	4 mm2
Range	±1g, ±2g
Maximum acceleration	500g

Table 1 summarizes the specification of the designed sensor and IC. Comparing with other digital accelerometers, this closed loop accelerometer has several advantages such as: low Brownian noise, high sensitivity, and small transverse sensitivity. By applying the sigma-delta modulation technique, this sensor can obtain lower quantized noise and digital output.

4. CONCLUSIONS

A specific sigma delta converter is designed in order to manufacture digital accelerometers from open loop sensors fabricated at ITIMS. The sigma delta modulator has the ability of interfacing to different capacitive sensor with optimized characterizes. The simulation result is very agreed with the theoretical prediction and it results in a closed loop accelerometer whose high sensitivity, low noise and digital output.

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